## REMARKS

Claims 1-14 are presented for examination. Claims 12 and 14 are found allowable subject to being rewritten in independent form.

REJECTION UNDER 35 U.S.C. 103

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kudo et al. on view of Geldman et al. This rejection is respectfully traversed for the following reasons.

In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to factually support a conclusion of obviousness. As stated in *Graham v. John Deere Co.* 383 U.S. 1, 13, 148 U.S.P.Q. 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art.

As demonstrated below, the Examiner has failed to ascertain the differences between the claims and applied references and thus to establish a *prima facie* case of obviousness.

Claim 1 recites a microprocessor including:

- a program control unit controlling fetch of an instruction code;

- an instruction decode unit decoding said fetched instruction code;

- an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

- a data operation unit operating data on the basis of the result of decoding by said instruction decode unit.

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The claim specifies that the data operation unit executes data transfer between registers and data transfer between said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

The Examiner admits that Kudo does not disclose the claimed data transfer between registers and data transfer between the registers and the memory in correspondence to single instruction code having a single operation code fetched by the program control unit. Geldman is relied upon for disclosing "a system including a single instruction having single opcode MV8 for transferring data between registers (e.g. see col. 8, lines 16-19)."

Considering Geldman, the reference discloses instruction MV8 for copying the contents of register b into register a (col. 8, lined 16-19).

By contrast, claim 1 recites execution of data transfer between registers and data transfer between the registers and the memory in correspondence to a single instruction code having a single operation code.

Hence, Geldman does not disclose the claimed data operation unit that executes data transfer between registers and data transfer between said registers and said memory in the manner required in claim 1.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. *Cable Electric Products, Inc. v. Genmark, Inc.*, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As neither Kudo nor Geldman discloses the claimed data operation unit that executes data transfer between registers and data transfer between said registers and said memory in the manner required in claim 1, a combination of Kudo with Geldman is not sufficient to arrive at the claimed invention.

In the absence of a teaching or suggestion in the references of the details recited in claim 1, it is submitted that the Examiner's conclusion of obviousness is not warranted. Applicant, therefore, respectfully submits that the rejection of claims 1-10 under 35 U.S.C. § 103 is improper and should be withdrawn.

REJECTION UNDER 35 U.S.C. 102

Claims 11 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kudo et al. This rejection is respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." *In re Schaumann*, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

As demonstrated below, Kudo neither expressly nor under principles of inherency discloses the claimed invention.

In particular, independent claim 11 recites an assembler including:

- a code reading unit reading a code from a source program;

- a storage unit storing information for specifying a plurality of registers;

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- a first code generation unit storing said information for specifying said plurality of registers included in said code read by said code reading unit in said storage unit and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

- a second code generation unit referring to said information for specifying said plurality of registers stored in said storage unit and generating a code to pop data stored in said plurality of registers when said code read by said code reading unit is a second macro instruction.

Independent claim 13 recites a storage medium, readable by a computer, on which an assembly program for making said computer execute an assembly method is recorded. The assembly method comprises the steps of:

- reading a code from a source program; - storing information for specifying a plurality of registers included in said code and generating a code to push data stored in said plurality of registers when said code is a first macro instruction; and

- referring to said stored information for specifying said plurality of registers and generating a code to pop data stored in said plurality of registers when said read code is a second macro instruction.

In the previous Request for Reconsideration, Applicant argued that Kudo does not disclose generating a code to push data stored in the plurality of registers when the code read from the source program is a first macro instruction, referring to the information for specifying the plurality of registers and generating a code to pop data stored in the plurality of registers when the read code read is a second macro instruction.

In response, the Examiner relies upon col. 14, lines 44-58 for disclosing the claimed features.

Considering the reference, Kudo discloses that the group of stack pointer instructions include "a sequential push instruction (pushn); and a sequential pop instruction (popn)" (col. 14, lines 44-53).

However, the reference does not disclose generating a code to push data stored in the plurality of registers when the code read from the source program is a first macro instruction, and generating a code to pop data stored in the plurality of registers when the read code is a second macro instruction, as claims 11 and 13 require.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

However, Kudo provides no reason for a person of ordinary skill in the art to conclude that a sequential push instruction (pushn) necessarily pushes data stored in the plurality of registers when the code read from the source program is a first macro instruction, and a sequential pop instruction (popn) necessarily pops data stored in the plurality of registers when the read code is a second macro instruction, as claims 11 and 13 require.

Accordingly, Kudo neither expressly nor under principles of inherency discloses generating a code to push data stored in the plurality of registers when the code read from the source program is a first macro instruction, referring to the information for specifying the plurality of registers and generating a code to pop data stored in the plurality of registers when the read code read is a second macro instruction.
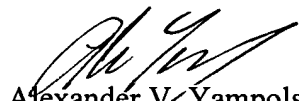
Hence, Kudo et al. does not describe the claimed invention within the meaning of 35 U.S.C. § 102. ***Kalman v. Kimberly-Clark Corp., supra***. Applicant, therefore, respectfully submits that the rejection of claims 11 and 13 under 35 U.S.C. § 102 as anticipated by Kudo et al. is untenable and should be withdrawn.

In view of the foregoing, and in summary, claims 1-14 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Alexander V. Yampolsky
Registration No. 36,324

600 13<sup>th</sup> Street, N.W.
Washington, DC 20005-3096
202.756.8000 SAB:AVY:men
Facsimile: 202.756.8087
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